Experimental Investigation of Ballistic Carrier Transport for Sub-100-nm Ge n-MOSFETs

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***Abstract*— We demonstrate an experimental study on the ballistic transport behavior of sub-100 nm GeOI n-MOSFETs, by adopting an ultrafast pulsed I–V system for measurement. High performance GeOI n-MOSFETs suffer severer self-heating effect and traps in the dc characterization process than in a "real" high-speed IC circuit. In this letter, the ballistic transport parameters for nanoscale Ge n-MOSFETs are extracted by the pulsed I–V method, and is compared with the SOI n-MOSFETs. The ballsiticity for Ge MOSFETs is higher than Si transistors at the same gate length L_G. Furthermore, the scalability of the ballistic parameters for Ge n-MOSFETs is modeled and predicted for the sub-10-nm technology nodes.**

***Index Terms*— Germanium MOSFETs, ballistic transport, pulsed IV, GeOI, self-heating effect.**

I. Introduction

AS THE technology node advances into sub-20 nm, further scaling of Si transistors becomes incredibly challenging. Higher mobility materials are explored as the potential alternatives to replace the Si channel. Germanium (Ge), owing to its very high carrier mobility, is considered as one of the promising channel materials for sub-10 nm applications [1]–[5]. Long-channel Ge MOSFETs with superior mobility and on-state current have been widely demonstrated [2], [3] while there are not so much work on short-channel Ge transistors, especially on the ballistic transport model for sub-100 nm Ge MOSFETs [4]–[7]. As transistors advance into nanoscales, the linear relationship between saturation drive current I_{Dsat} and L_G^{-1}, does not hold for sub-100 nm transistors. A ballistic transport model has been well established to study the ballistic characteristics of nanoscale Si MOSFETs [8]. However, due to the lack of nanoscale Ge MOSFETs with decent performance, there are not so much experimental work on the ballistic transport characterization of Ge devices.

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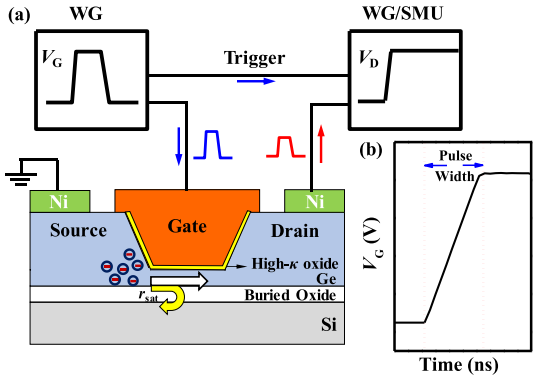

Fig. 1. (a) The schematics of a Ge MOSFET fabricated on a GeOI substrate. The layout of a pulsed IV testing system is also illustrated. Pulsed signals are input at the gate and drain electrodes while the source electrode is kept ground. (b) The waveform of V_G used for the I_D-V_G characterization.

In this work, an ultrafast pulsed IV measurement system is adopted to characterize the ballistic transport parameters of sub-100 nm Ge n-MOSFETs (Fig. 1). For transistors fabricated on Ge-on-insulator (GeOI) substrates, self-heating effect (SHE) would be severe if characterized using traditional DC method, due to the very low thermal conductivity of thin-film Ge and buried oxide [9]. In addition, by using the DC method, the large number of traps in the dielectric/Ge channel interface may affect the accuracy in the ballistic parameter extraction. Whereas, in the pulsed IV measurement, the ultrashort pulse width ($\sim$ 100 ns) may only lead to negligible heat generated in the Ge channel [10]. Furthermore, since the traps might not be able to follow the measurement speed, they could remain unfilled during the pulsed measurement [11]. In this letter, the ballistic transport characterization for Ge MOSFETs using both DC and ultrafast pulsed IV methods are compared. Based on the experimental results, the ballistic transport parameters for Ge and Si n-MOSFETs are compared. The scalability of ballistic efficiency B_{sat} is also modeled and predicted for sub-10 nm technology nodes.

II. Device Fabrication and Characterization

GeOI wafer with lightly n-type doped (100) Ge was used for device fabrication. A hard mask was used to define the device channel ranging from 50 nm to 100 nm. Recessed

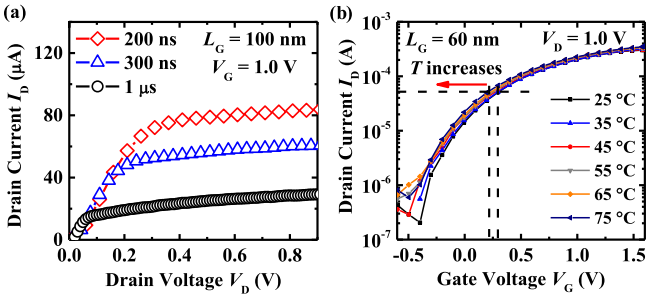

Fig. 2. (a) I_D-V_D plot for a GeOI MOSFET with $L_G = 100$ nm measured by pulsed IV method. Constant V_G of 1.0 V and pulsed V_D with pulse width ranging from 200 ns to 1 μs were used as the gate and drain bias conditions, respectively. (b) I_D-V_G plots for a GeOI n-MOSFET with $L_G = 60$ nm measured at various temperatures, using pulsed IV method (constant V_D and pulsed V_G).

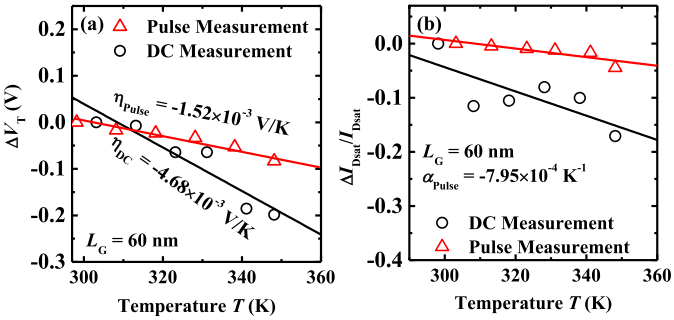

Fig. 3. (a) The change of V_T and (b) $\Delta I_{Dsat}/I_{Dsat}$ as a function of characterization T for a MOSFET with $L_G = 60$ nm measured by both DC (circle) and pulsed IV (triangle) methods, respectively.

channel dry etch was then performed to achieve a channel thickness of 25 nm. After the surface cleaning, a two-step deposition process was adopted to grow 9 nm-thick Al_2O_3 as the gate dielectric. After recessed S/D dry etching, Ni was deposited to form the S/D contacts followed by the gate metal deposition. A detailed description on the process flow was provided in [12].

Commercial pulsed IV measurement system was used for the electrical characterization. Devices with L_G ranging from ~50 nm to 100 nm were characterized at various temperatures T ranging from ~298 K (25 °C) to ~348 K (75 °C).

The drive current is related to the carrier transport parameters, namely, carrier injection velocity v_{inj} and ballistic efficiency B_{sat} by $I_{Dsat} = W v_{inj} B_{sat} C_{ox}(V_G - V_T)$, where C_{ox} is the oxide capacitance, W is channel width, and V_T is the threshold voltage [8]. Based on the equation, a temperature dependent I-V technique was developed and used to determine backscattering parameters of sub-100 nm devices as follows,

$$\frac{\lambda_o}{l_o} = (2c+1)\left[\frac{1}{2} - \left(\alpha + \frac{\eta}{V_G - V_T}\right)\right]^{-1} - 2, \qquad (1)$$

where c is a constant, λ_o is the near-equilibrium mean-free path, l_o is the critical distance over which the potential drops by $k_B T$ from the peak of the conduction band barrier [as illustrated in Fig. 4(b)], η and α are defined to be the slopes of V_T shift ΔV_T and $\Delta I_{Dsat}/I_{Dsat}$ with respective to temperature T, respectively. From the extracted λ_o/l_o, B_{sat} can be calculated using

$$B_{sat} = \frac{1}{1 + 2(l_o/\lambda_o)}, \qquad (2)$$

If the carriers injected from the source end do not experience any scattering when reaching the drain end, $B_{sat} = 1$.

III. Results and Discussion

Fig. 2(a) shows the drain current-drain voltage (I_D-V_D) plot for a GeOI n-MOSFET with $L_G = 100$ nm measured by the pulsed IV method. Constant V_G of 1.0 V and pulsed V_D with pulse width ranging from 200 ns to 1 μs were used as the gate and drain bias conditions, respectively. As the pulse width increases, I_D degrades significantly, showing severe SHE of GeOI devices when measurement time or pulse width is longer. Therefore, when using DC method for the carrier transport characterization, the large heat generated in the channel region will introduce extra phonon scattering, and degrade the carrier transport parameters, as compared to those in "real" high speed IC circuits.

To extract the ballistic transport parameters for Ge devices, the I_D-V_G characteristics were measured at various temperatures, by both the DC and pulsed IV methods, respectively. Fig. 2(b) is the I_D-V_G characteristics of a Ge n-MOSFET with $L_G = 60$ nm, measured from 25 °C to 75 °C using pulsed IV measurement. The pulse width for the I_D-V_G measurement in Fig. 2(b) is 200 ns. V_T is taken by constant current method while I_{Dsat} is taken at $V_G = V_T + 1.0$ V. It is shown that as T increases, the bandgap and surface potential decrease, therefore, V_T decreases. Fig. 3(a) and (b) shows the change of ΔV_T and $\Delta I_{Dsat}/I_{Dsat}$ as a function of T, respectively, for a Ge n-MOSFET with $L_G = 60$ nm, measured by both the DC and pulsed IV methods. Due to the severe SHE in the DC measurement, the actual channel T is higher than the characterization/substrate T, therefore, the ΔV_T extracted from the DC measurement is higher than that from the pulse measurement, leading to a larger value of η. Similarly, the change of $\Delta I_{Dsat}/I_{Dsat}$ is also smaller for device measured by the pulsed IV method. It should be noted that for Ge transistors, there are large quantities of traps in the Ge gate stack. When characterizing their electrical properties using the pulse method, the traps in the gate stack may not follow the very fast pulse and remain unfilled [11]. Therefore, as compared with the DC method, the traps would less likely affect the ballistic transport behaviors in the Ge devices. The interference of traps for longer characterization time could partially explain the large scattering of $\Delta I_{Dsat}/I_{Dsat}$ observed in the DC measurement, in Fig. 3(b). For the Ge devices in Fig. 3, α_{pulse} is -7.95×10^{-4} K^{-1} and η_{pulse} is -1.52×10^{-3} V/K which are much smaller than the corresponding parameters extracted from the DC measurement.

The ballistic transport models for Ge and Si MOSFETs are similar but the constant c used in Eq. 1 for Ge is different from that for Si. Actually, c is the exponent which correlates the low field mobility and temperature. For Si, μ_{Si} is proportional to $T^{-1.5}$. Therefore, $c_{Si} = 1.5$ [13]. In this work, we use Monte-Carlo method to calculate the temperature exponent for Ge mobility μ_{Ge}, as shown in Fig. 4(a) where $c_{Ge} = 1.92$.

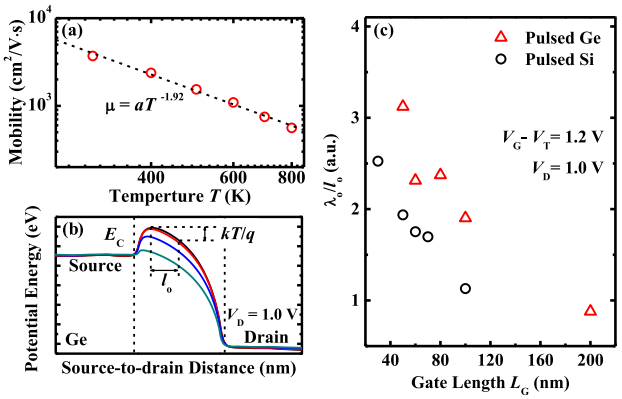

Fig. 4. (a) The electron mobility decreases exponentially as the temperature increases. (b) Conduction band profile from source-to-drain direction for the same Ge MOSFET as shown in (a). (c) Comparison of λ_o/l_o ratio for Ge and Si MOSFETs at various L_G.

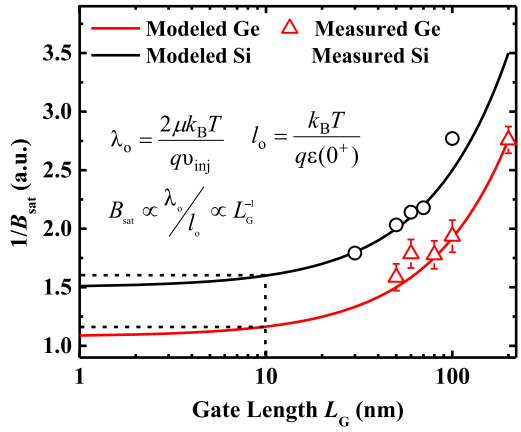

Fig. 5. The change of $1/B_{sat}$ is modelled as a function of L_G for undoped GeOI and SOI n-MOSFETs. Experimentally extracted B_{sat} for both groups of devices are provided for comparison with the numerically simulated curves.

A detailed description on the simulation process for Ge mobility was reported in [14]. As c_{Ge} is higher than c_{Si}, theoretically, the λ_o/l_o ratio is higher for Ge than that for Si, for transistors at the same L_G. Fig. 4(b) shows the change of conduction band profiles as V_G increases. λ_o/l_o ratio would increase as l_o is shorter for higher V_G. Fig. 4(c) compares the λ_o/l_o ratio for GeOI and SOI n-MOSFETs (reported in [15]) both measured by pulsed IV method. For both transistors, the channel is undoped. It could be observed that, as L_G decreases, λ_o/l_o for both groups increases since l_o is reduced for devices with smaller L_G. In addition, at the same L_G, λ_o/l_o ratio for Ge is higher. The root cause of the phenomenon is λ_o for Ge is longer than Si. Therefore, from the perspective of dimension evolution, it is earlier for Ge MOSFETs to enter the quasi-ballistic transport regime.

Since B_{sat} is inversely proportional to L_G [16], the scalability of B_{sat} for GeOI and SOI n-MOSFETs is modelled as a function of L_G as shown in Fig. 5. Experimentally extracted B_{sat} for both groups of devices are provided which fit well with the numerically simulated curves. Ge transistors show higher ballistic efficiency than Si MOSFETs at the same L_G. It could be interpreted from Fig. 5 that at $L_G = 10$ nm, B_{sat} for Ge devices measured by the pulsed IV method could reach 0.85 while that for Si devices is 0.62. However, for a reduced V_G and V_D in the future technology node, B_{sat} would be smaller than our predictions in Fig. 5. A higher B_{sat} indicates a higher I_{Dsat} even if V_G is unchanged. Furthermore, a higher B_{sat} indicates a more temperature-independent carrier transport. Therefore, for Ge transistors, a more ballistic device leads to less V_T and I_{Dsat} degradation at high operation temperature, resulting in less reliability considerations for circuit designs.

IV. Conclusion

In this letter, we experimentally investigated the ballistic transport behavior of Ge n-MOSFETs fabricated on GeOI substrate. A novel pulsed IV testing method was exploited for the electrical characterization of Ge n-MOSFETs. Due to the low thermal conductivity of thin-film Ge and buried oxide, Ge transistors suffer much higher SHE in the traditional DC testing process than that in a "real" high speed IC circuit. The pulsed IV method could eliminate the SHE and trap effects in the characterization process, which results in accurate extraction of ballistic transport parameters. It is demonstrated both theoretically and experimentally that the ballistic efficiency of Ge n-MOSFETs is higher than that of Si transistors. Furthermore, based on the numerical model, the value of B_{sat} for Ge devices would be higher for sub-10 nm technology node.

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